



UNITED STATES PATENT AND TRADEMARK OFFICE

11A
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,936	09/09/2003	Richard M. Fastow	AMD-H0561	3102
7590	07/27/2006		EXAMINER	
WAGNER, MURABITO & HAO LLP Third Floor Two North Market Street San Jose, CA 95113			NGUYEN, DAO H	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,936	FASTOW ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 June 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,8,10,12,21-23 and 25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,8,10,12,21-23 and 25 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the communications dated 06/07/2006, claims 1, 8, 10, 12, 21-23, and 25 are active in this application.

Claims 2-7, 9, 11, 13-20, and 24 have been cancelled.

Remarks

2. Applicant's argument(s), filed 06/07/2006, with respect to the final rejection of claims 1, 8, 10, 12, 21-23 and 25 have been fully considered. However, reformation and corrections to such rejection are made below to further clarify the similarities between the applied references and the pending claimed subject matter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim(s) 1, 8 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,784,480 to Bhattacharyya.

Regarding claim 1, Bhattacharyya discloses a flash memory cell, as shown in figs. 1, 8, 14, 17, and 18, comprising:

a substrate 102 comprising source and drain regions 104, 106;

a silicon dioxide layer 122 adjoining said substrate 102;

a polysilicon floating gate 118 (it is noted that fig.1 of Bhattacharyya, for example, shows a floating gate layer 118 made of silicon (col. 6, lines 41-42); definitely, a silicon layer may be a monosilicon layer or a polysilicon layer; both “monosilicon” and “polysilicon” are comprised in the meaning of “silicon”; furthermore, col. 14, line 23 discusses about a floating gate being a polysilicon floating gate; therefore, it is inherent that the silicon floating gate discussed on col. 6, lines 41-42 and illustrated in fig. 1 can be a polysilicon floating gate);

a dielectric layer 124 (fig. 1) or 1850&1856 (fig. 18) sandwiched between and adjoining both said silicon dioxide layer 122 and said floating gate 118, said dielectric layer 124 comprising a dielectric material (Ta_2O_5) having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (see col. 4, lines 26-40; col. 6, lines 23-5);

an oxide-nitride-oxide (ONO) layer 128 adjoining said floating gate 118; and

a control gate 114 adjoining said ONO layer 128.

Regarding claim 8, Bhattacharyya disclose the flash memory cell wherein said dielectric layer 1850&1856 (fig. 18) comprises a composite of said metal oxide 1850 and a material 1856 selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See further col. 11, line 57 to col. 14, line 9.

5. Claim(s) 10 and 12 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,348,380 to Weimer et al.

Regarding claim 10, Weimer discloses a flash memory array comprising memory cells, wherein a memory cell comprises:

a substrate 220 comprising a source and a drain (col. 5, lines 32-37);
a first layer (layer 290b and portion of layer 292 along the side of layer 290b, fig. 12) comprising a silicon material (see col. 12, lines 22-40);
a tunnel oxide layer 230 (figs. 8-10) or 230' (fig. 12) sandwiched between and adjoining both said substrate 220 and said first layer 290b&292, said tunnel oxide layer 230/230' comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (Ta_2O_5 , col. 6, lines 29-34);
a polysilicon floating gate 250 (col. 6, lines 54-63) adjoining said first layer 290b&292;
an oxide-nitride-oxide (ONO) layer 260 adjoining said floating gate 250 (figs. 7-9); and
a control gate 270 adjoining said ONO layer 260.

Regarding claim 12, Weimer discloses the flash memory array wherein said silicon material (layer 290b and portion of layer 292 along the side of layer 290b, fig. 12) is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 12, lines 22-40.

6. Claim(s) 21-23 and 25 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,559,007 to Weimer.

Regarding claim 21, Weimer discloses a flash memory cell, as shown in figs. 1, 2, comprising:

a substrate 20 comprising a source 22 and a drain 24;
a first layer (layer 90a and part of layer 92 along the side of layer 90a) comprising a first silicon material and adjoining said substrate 20 (see fig. 2 and col. 5, lines 27-54);
a second layer (layer 90b and part of layer 92 along the side layer 90b)
comprising a second silicon material (fig. 2 and col. 5, lines 27-54);
a dielectric layer 30&40 sandwiched between and adjoining both said first layer and said second layer, said dielectric layer 30&40 comprising a dielectric material (Ta_2O_5) having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (layer 30 comprising Ta_2O_5 and layer 40 is a nitridation of layer 30);
a polysilicon floating gate 50 adjoining said second layer (fig. 1 of Bhattacharyya, for example, shows a floating gate layer 118 made of silicon (col. 6, lines 41-42);

definitely, a silicon layer may be a monosilicon layer or a polysilicon layer; both "monosilicon" and "polysilicon" are comprised in the meaning of "silicon"; furthermore, col. 14, line 23 discusses about a floating gate being a polysilicon floating gate; therefore, it is inherent that the silicon floating gate discussed on col. 6, lines 41-42 and illustrated in fig. 1 can be a polysilicon floating gate);

an oxide-nitride-oxide (ONO) layer 60 adjoining said floating gate 50; and
a control gate 70 adjoining said ONO layer 60. See further col. 4, line 3 to col. 6, line 65.

Regarding claim 22, Weimer discloses the flash memory cell wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See fig. 2 and col. 5, lines 27-54.

Regarding claim 23, Weimer discloses the flash memory cell wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See fig. 2 and col. 5, lines 27-54.

Regarding claim 25, Weimer discloses the flash memory cell wherein said dielectric layer 30&40 comprises a composite of said a metal oxide (Ta_2O_5) and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 4, line 3 to col. 6, line 59.

7. Claim(s) 21 is rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,693,321 to Zheng et al.

Regarding claim 21, Zheng discloses a flash memory cell, as shown in figs. 1, 8, comprising:

a substrate 12 comprising a source 16 and a drain 16;
a first layer (left layer 34) comprising a first silicon material (col. 7, lines 50-53) and adjoining said substrate 12;
a second layer (right layer 34) comprising a second silicon material (col. 7, lines 50-53);
a dielectric layer 20 sandwiched between and adjoining both said first and said second layers 34, said dielectric layer 20 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (col. 7, lines 5-14 and col. 7, line 66 to col. 8, line 51);
a polysilicon floating gate 18 (col. 7, lines 15-19) adjoining said second layer an oxide-nitride-oxide (ONO) layer 24 adjoining said floating gate 18; and
a control gate 32 adjoining said ONO layer 24.

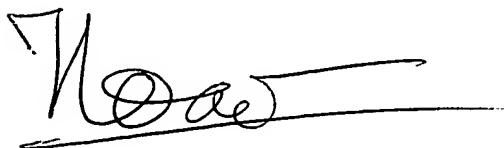
Conclusion

8. THIS ACTION IS MADE FINAL. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action

and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



DOUGLAS W. OWENS
PRIMARY EXAMINER

Dao H. Nguyen
Art Unit 2818
July 12, 2006